UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,957	03/22/2002	Wolfgang Fey	AP9722	2651

10291 7590 07/26/2004

RADER, FISHMAN & GRAUER PLLC
39533 WOODWARD AVENUE
SUITE 140
BLOOMFIELD HILLS, MI 48304-0610

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	7

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,957	FEY ET AL.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-21* is/are rejected.

7)☒ Claim(s) *22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Preliminary Amendment filed March 22, 2002. Claims 1-12 are cancelled. Claims 13-24 are pending and are hereby presented for examination.

Drawings

2. The drawings are objected to because the functional blocks, in FIGS. 1, 2 and 5, require descriptive legends without having to refer back to the specification. Suitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing. They should contain as few words as possible.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13, 14, 16 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Traynor (US 4710934).

Regarding independent Claims 13, 19, Traynor discloses a method and apparatus for an error detection/correction Random Access Memory (RAM) module for storing coded data words, FIG. 1, comprising:

A first circuit unit parity array (12) for producing a check bit word (parity information), which is generated in accordance with a block code error algorithm from the coded data words associated with a (collective data word portion) stored in an information array (10) when writing and reading the coded data words into / from the RAM module, (SUMMARY OF THE INVENTION).

A second circuit unit for regenerating the check bit word (parity information) from the read-out coded data words, using error syndrome/parity generator (48) which also operates in a parity mode to receive the collective data

portion of the coded data word and generate new parity information, and

generating an error message using the error position decode circuit 52 to determine which, if any, bits in the coded data word on the buses (34 and 40) are in error by comparing the read-out check bit word from the RAM on the buses (34 and 40) with the regenerated check bit word from the error syndrome/parity generator (48).

Regarding Claim 14, Traynor discloses parity array (12) for producing a check bit word (parity information) by determining parity bits.

Regarding Claim 16, Traynor discloses check bit word using parity array (12) generated from a plurality of data words stored in the associated information array (10) and parity bits of the check bit word are respectively determined from equal digits of all data words, as shown in Table 2 and FIG. 2, which illustrates the arrangement of data and parity bits stored in the memory.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traynor (US 4710934) in view of Cislaghi et al. (US 3972033).

Regarding Claims 15, 20, Traynor does not explicitly disclose a 2-bit parity word generated from each data word, and one parity bit is respectively determined from each half of the data word. Cislaghi et al. (US 3972033) discloses a parity check system in a semiconductor memory wherein recording words comprising 16 information bits, and are divided into two "bytes", of eight bits each. Each byte is provided with its own check bit and two half-words of nine bits are recorded at the same address (see ABSTRACT and SUMMARY OF THE INVENTION). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use 16 bit data words divided into two "bytes", with each byte having its own corresponding check bit, as taught by Cislaghi, in the error detection / correction method and apparatus of Traynor, thus making possible the detection of errors due to a false addressing, causing the whole word, and its check bit, to be written at a wrong address.

6. Claims 17, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traynor (US 4710934) in view of Hancock (US 4277844).

Regarding Claims 17, 18, Traynor does not explicitly disclose generating check bit words by calculating CRC words, wherein a memory word is formed by summing a plurality of data words, and wherein an associated CRC word is calculated. Hancock (US 4277844) discloses a method (FIG. 5) comprising information data bits being transmitted to a memory by an external source, such as a central processing unit. The method further including a step of generating 8 check bits word and a next step for storing the word and generating a cyclic

redundancy character (CRC), wherein during the write operation, the CRC division is performed, yielding 5 bytes of CRC data which are stored at the end of the record, this being the last step of the write operation. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the cyclic redundancy character (CRC) generating method steps, as taught by Hancock, in the method and apparatus of Traynor, so as to provide an improved data error detection and correction method by saving the location of the most recently identified error location.

Regarding Claim 21, Traynor does not explicitly disclose determining the number of registers by including one CRC register for each four data words. Hancock shows in FIG. 4 a typical layout of a memory device comprising Data bits with the associated cyclic redundancy check (CRC) bits. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use layout of the memory device, as taught by Hancock, in the method and apparatus of Traynor so as to provide an improved data error detection and correction method by saving the location of the most recently identified error location.

Allowable Subject Matter

7. Claims 22-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention, Regarding Claim 22, of a circuit configuration including a multiplexer for storing four data words as one memory word, and a CRC arithmetic unit for calculating the CRC word from a memory word and for storing the CRC word in an associated CRC register.

Claim 23 depends from claim 22, and is allowable.

Regarding Claim 24, a circuit configuration including a global check bit word register for storing a global check bit word, the bits of which are respectively determined from equal digits of all data words, and an associated register for storing a check bit word which is determined from the contents of the global register.

Conclusion

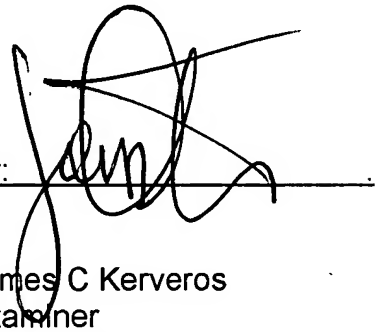
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 2 July 2004
Office Action: Non-Final Rejection

By: 

James C Kerveros
Examiner
Art Unit 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner